REMARKS

Claims 1-8 are pending. Claims 1 and 5 are independent.

The Final Office rejected claims 1-8 under 35 U.S.C 112, second paragraph, as being indefinite. In particular, that "it is indefinite as to how, or if, the pipeline registers that are "between any two of said clusters with a dedicated direct signal data signal connection there between" are the same as the "one or more additional pipeline registers" arranged in the control connections. In the instant disclosure (particularly page 4, lines 18-29 which have been cited by applicant), the pipeline register that is arranged in the control connection paths, in order to pipeline the control signals, is not described as being between any two of the clusters." (Office Action, paragraph 4)

In response, independent claims 1 and 5 have been amended to recite the limitations of: "…one or more pipeline registers arranged in both said control connections, depending on the distance between said instruction unit and said clusters, and in a dedicated direct signal data signal connection between any two of said clusters."

Support for these amendments can be found, *inter alia*, in FIG. 1 and on page 4, lines 18-29:

> "In Fig. 1 a clustered VLIW architecture with a full point-to-point connectivity topology according to a first embodiment is shown. The architecture includes four clusters, namely clusters A, B, C and D, which are fully connected to each other and an instruction fetch/dispatch unit IFD being connected to each cluster A-D via control connections paths CA-CD. Accordingly, **there is always a dedicated direct data signal connection present between any two clusters with pipeline registers P arranged between each two clusters.** The latency of an inter-cluster transfer of data is always the same for every inter-cluster connection independent of the actual distance between the clusters on the chip. The actual distance on the chip between the clusters A and C, and clusters B and D is considered to be longer than the distance between the clusters A and D, A and B, B and C, as well as C and D. Therefore**, a pipeline**

register P is arranged in the control connection paths CC and CD, in order to pipeline the control signals to remote clusters C, D." (Emphasis Provided).

Moreover, as shown in FIG. 1-4, there are pipeline registers in both the control connection paths CA, CB, CC and CD, as well as pipeline registers in the dedicated direct signal data signal connections (unlabeled) between any two clusters.

Accordingly, and for at least the reasons set forth in above, Applicants respectfully submit that the claims are well within the requirements of 35 U.S.C. § 112, ¶ 2. Therefore, Applicants respectfully submit the rejection can no longer be sustained.

With regard to claims 2-16 and 18-26 these claims depend from the independent claim discussed above, which has been shown to be allowable in view of the cited reference. Accordingly, each of claims 2-16 and 18-26 are also allowable by virtue of its dependence from an allowable base claim.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. Entry of this amendment and a Notice of Allowance is respectfully requested.

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